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10/015,180	11/16/2001	Manish Jain	SNSY-A2001-001	7199

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BEVER, HOFFMAN & HARMS, LLP
1432 CONCANNON BLVD
BLDG G
LIVERMORE, CA 94550-6006

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,180	JAIN ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11/16/01 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 were examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 23-32 and 39-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The word "system" renders the claims ambiguous since a system is similar to a method and/or apparatus. Examiner suggest changing system to apparatus.

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-~~12~~ 14 are rejected under 35 U.S.C. 103 (a) as obvious by Pillage et al (U.S. Patent 5,379,231 (1995)) in view of Gamal et al., (U.S. Patent 5,754,826 (1998)). Pillage et al., teaches a method for simulating a microelectronic circuit with moments; these moments are used to calculate the poles and residues for a given node and generate an approximate model; but doesn't teach timing constraints. Pillage et al., teaches a single design and development process to be conducted for ICs fabricated under different process (abstract) with timing constraints (column 13, lines 49-55).

At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Pillage et al., by way of Gamal et al. simulate the IC design using models for each target process to ensure that the resulting IC will meet the design specification under typical, worst or best case conditions (column 3, lines 20-25).

Claim 1. A method for enhancing dynamic timing simulation (Pillage: title; Gamal: column 3, lines 35-40) comprising: accessing a netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8) comprising combinational logic nodes, including output nodes, interconnection (Gamal: column 7, lines 60-65), and input and output storage

elements; assigning a delay to each of said nodes; determining a maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum for each node; determining a safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period for each of said output nodes (within min/max parameter; Gamal: column 7, lines 39-46); removing timing checks from those output nodes for which the maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum is less than the safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period; determining a minimum reverse delay difference for each of a portion of said nodes (within min/max parameter; Gamal: column 7, lines 39-46); identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum; setting the delays for the identified nodes to zero (inherent feature of logic functions as well as simulation); and performing dynamic timing simulation (Pillage: title; Gamal: column 3, lines 35-40).

Claim 2. The method of claim1, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein the forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) maximum delay (Gamal: column 7, lines 40-45) sum includes an interconnect (Gamal: column 7, lines 60-65) delay.

Claim 3. The method of claim 1 (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein the delay assigned to at least one said nodes is derived from a gate delay.

Claim 4. The method of claim 1, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein the fundamental unit for deriving the node delays is a gate.

Claim 5. The method of claim 1, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein at least one of said output nodes is associated with a sequential element.

Claim 6. The method of claim 5, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein said sequential element is a flip-flop (Gamal: column 2, lines 10-13).

Claim 7. The method of claim 6, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; Gamal: column 2, lines 10-13) further including the setting zero (inherent feature of logic functions as well as simulation) of delays associated with clock circuit buffers driving said flip-flop (Gamal: column 2, lines 10-13).

Claim 8. The method of claim 5, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein said safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period is derived from a clock period minus a setup time.

Claim 9. The method of claim 1, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) further including accessing a standard delay format (SDF) (Gamal: column 7, lines 34-35) file to obtain delay information.

Claim 10. The method of claim 9, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein said delay information relates to data dependent delays.

Claim 11. The method of claim 1, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) further including setting the clock-to-Q delay to zero (inherent feature of logic functions as well as simulation) for input storage elements that have had the delays of all connected nodes set zero (inherent feature of logic functions as well as simulation).

Claim 12. A computer (Gamal: column 14, lines 38-40) readable medium containing executable instructions which, when executed processing system, causes the system to

perform the steps for enhancing the runtime speed logic simulator, comprising: logic circuit as a defining a combinational portion of a network comprising nodes, including output nodes, interconnect (Gamal: column 7, lines 60-65)ions, and input and output storage elements; assigning a determining delay to each of said nodes; a maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum for each node; determining a safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period for each of said output nodes; removing timing the maximum checks from those output nodes for which forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum is less than the safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period; determining a minimum reverse of a portion of said nodes; delay difference for each portion of said nodes; identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum; setting the delays for the identified nodes to zero (inherent feature of logic functions as well as simulation); and compiling the logic simulator.

Claim 13. The computer (Gamal: column 14, lines 38-40) readable medium of claim 12, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45)wherein the forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) maximum delay (Gamal: column 7, lines 40-45) sum includes an interconnect (Gamal: column 7, lines 60-65) delay;

Claim 14. The computer (Gamal: column 14, lines 38-40) readable medium of claim 12, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45)wherein the delay assigned to at least one of said nodes is a gate delay.

Claim 15. The computer (Gamal: column 14, lines 38-40) readable medium of claim 12, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein the fundamental unit for deriving the node delays is a gate.

Claim 16. The computer (Gamal: column 14, lines 38-40) readable medium of claim 12, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein at least one of said output nodes is associated with a storage element.

Claim 17. The computer (Gamal: column 14, lines 38-40) readable medium of claim 16, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein said storage element is a flip-flop (Gamal: column 2, lines 10-13).

Claim 18. The computer (Gamal: column 14, lines 38-40) readable medium of claim 17, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) further including instructions for to zero (inherent feature of logic functions as well as simulation) delays associated with clock circuit buffers driving said flip-flop (Gamal: column 2, lines 10-13).

Claim 19. The computer (Gamal: column 14, lines 38-40) readable medium of claim 12, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) wherein said safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period is derived from a clock period and a setup time.

Claim 20. The computer (Gamal: column 14, lines 38-40) readable medium of claim 19, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) further including instructions for accessing a standard delay format (SDF) (Gamal: column 7, lines 34-35) file to obtain delay information.

Claim 21. The method of claim 20, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; Gamal: column 14, lines 38-40) wherein said delay information relates to data dependent delays.

Claim 22. The computer (Gamal: column 14, lines 38-40) readable medium of claim 19, (Pillage: title; Gamal: column 3, lines 35-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) further including instructions for setting the clock-to-Q delay to zero (inherent feature of logic functions as well as simulation) for input storage elements that have had the delays of all connected nodes set to zero (inherent feature of logic functions as well as simulation).

Claim 23. The system for enhancing the runtime speed of a logic simulator comprising a computer (Gamal: column 14, lines 38-40) system, said computer (Gamal: column 14, lines 38-40) system further comprising instructions for: defining a combinational portion of a logic circuit as a network comprising nodes, including output nodes, interconnections (Gamal: column 7, lines 60-65), and input and output storage elements; assigning a delay to each of said nodes; determining a maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum for each node; determining a safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period for each of said output nodes; removing timing checks from those output nodes for which the maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) delay sum is less than the safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period; determining a minimum reverse delay difference for each of said interior nodes and said input nodes(within min/max parameter; Gamal: column 7, lines 39-46); identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-

45) delay sum; setting the delays for the identified nodes to zero (inherent feature of logic functions as well as simulation); and compiling the logic simulator.

Claim 24. The system of claim 23, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein the forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) maximum delay (Gamal: column 7, lines 40-45) sum includes an interconnect (Gamal: column 7, lines 60-65) delay.

Claim 25. The system of claim 23, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein the delay assigned to at least of said nodes is from a gate delay.

Claim 26. The system of claim 23, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein the fundamental unit deriving the node delays gate.

Claim 27. The system of claim 23, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein at least one said output nodes is associated with a storage element.

Claim 28. The system of claim 27, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said storage element is a flip-flop (Gamal: column 2, lines 10-13).

Claim 29. The system of claim 28, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said computer (Gamal: column 14, lines 38-40) system comprises instructions for setting to zero (inherent feature of logic functions as well as simulation) of delays associated with clock circuit buffers driving said flip-flop (Gamal: column 2, lines 10-13).

Claim 30. The system of claim 23, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said safe delay (within min/max parameter; Gamal: column 7, lines 39-46) period is derived from a clock period and a setup time.

Claim 31. The system of claim 23, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said computer (Gamal: column 14, lines 38-40) system comprises instructions for accessing a standard delay format (SDF) (Gamal: column 7, lines 34-35) file to obtain delay information.

Claim 32. The method of claim 31, (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said delay information relates to data dependent delays.

Claim 33. A method of performing dynamic simulation (Pillage: title; Gamal: column 3, lines 35-40) comprising: a) performing a delay assessment on a netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8) comprising gates and sequential cells, said delay assessment assigning delay information for respective nodes in said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8); b) removing timing checks on sequential elements indicated as exempt from timing checks based on said delay information; assigning zero (inherent feature of logic functions as well as simulation) delay to certain gates based on said delay information; and d) performing dynamic simulation (Pillage: title; Gamal: column 3, lines 35-40) on said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8), wherein said dynamic simulation (Pillage: title; Gamal: column 3, lines 35-40) enhances performance by: performing cycle based simulation (Pillage: title; Gamal: column 3, lines 35-40) with respect to assigned thereto zero (inherent feature of logic functions as well as simulation) delay as indicated by gates having and skipping timing checks for exempt sequential elements as indicated by b).

Claim 34. A method as described in Claim 33 (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal:

column 7, lines 39-46) wherein said delay information indicates a maximum delay (Gamal: column 7, lines 40-45) at each node.

Claim 35. A method as described in Claim 33 (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said delay assessment comprises: a1) at each input node of said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8), starting with a zero (inherent feature of logic functions as well as simulation) delay and traversing forward (Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) of said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8); and a2) during said traversing, aggregating maximum delays (Gamal: column 7, lines 40-45) and assigning aggregated maximum delays (Gamal: column 7, lines 40-45) to each node of each circuit path.

Claim 36. A method as described in Claim 33 (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein a) comprises determining exempt sequential elements by identifying output nodes each having a respective aggregated maximum delay (Gamal: column 7, lines 40-45) is less than a clock period minus a respective setup delay.

Claim 37. A method as described in Claim 36 (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein c) comprises: for each circuit path terminating at an exempt sequential element traversing backward through such circuit path to determine a partial circuit path for which zero (inherent feature of logic functions as well as simulation) delay can be designated to all gates therein.

Claim 38. A method as described in claim 37 (Gamal: column 14, lines 38-40; Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45; within min/max parameter; Gamal: column 7, lines 39-46) wherein said traversing backward comprises: starting with said clock period minus said setup delay at an exempt sequential cell; for each node traversed backward, subtracting a gate delay and assigning a lowest delay result value to said each node; and continuing to traverse backward only if said value is greater than said node's aggregate maximum delay (Gamal: column 7, lines 40-45).

Claim 39. A system comprising a processor coupled to a bus and memory coupled to said bus wherein said memory contains instructions that when executed on said processor implements a method of performing dynamic simulation (Pillage: title; Gamal: column 3, lines 35-40), said method comprising: a) performing a delay assessment on a netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8) comprising gates and sequential cells, said delay assessment assigning delay information for respective

nodes in said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8); b) removing timing checks on sequential elements indicated as exempted from timing checks based on said delay information; assigning zero (inherent feature of logic functions as well as simulation) delay to certain gates based on said delay information; and performing dynamic simulation (Pillage: title; Gamal: column 3, lines 35-40) on said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8), wherein said dynamic simulation (Pillage: title; Gamal: column 3, lines 35-40) enhances performance by: performing cycle-based simulation (Pillage: title; Gamal: column 3, lines 35-40) with respect to gates having assigned thereto zero (inherent feature of logic functions as well as simulation) delay as indicated by; and skipping timing checks for exempt sequential elements as indicated by b).

Claim 40. A system as described in claim 39, (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8; Pillage: title; Gamal: column 3, lines 35-40; Gamal: column 3, lines 35-40) wherein said delay information indicates a maximum delay (Gamal: column 7, lines 40-45) at each node.

Claim 41. A system as described in claim 39, (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8; Pillage: title; Gamal: column 3, lines 35-40; Gamal: column 3, lines 35-40) wherein said delay assessment comprises: a1) at each input node of said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8), starting with a zero (inherent feature of logic functions as well as simulation) delay and traversing forward

(Pillage: column 12, lines 5-10; Gamal: column 7, lines 35-45) through each circuit path of said netlist (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8); and a2) during said traversing, aggregating maximum delay (Gamal: column 7, lines 40-45)s and assigning aggregated maximum delays (Gamal: column 7, lines 40-45) to each node of each circuit path.

Claim 42. A system as described in claim 39 (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8; Pillage: title; Gamal: column 3, lines 35-40; Gamal: column 3, lines 35-40) wherein a) comprises determining exempt sequential elements by identifying nodes each having a respective aggregated maximum delay (Gamal: column 7, lines 40-45) that is less than a clock period minus a respective setup delay.

Claim 43. A system as described in claim 43 (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8; Pillage: title; Gamal: column 3, lines 35-40; Gamal: column 3, lines 35-40; Gamal: column 7, lines 40-45) where in c) comprises: for each circuit path terminating at an exempt sequential element, traversing backward through such circuit path to determine a partial circuit path for which zero (inherent feature of logic functions as well as simulation) delay can be designated to all gates therein.

Claim 44. A system as described in claim 43 (Pillage: column 7, lines 20-26; Gamal: column 8, lines 5-8; Pillage: title; Gamal: column 3, lines 35-40; Gamal: column 3, lines 35-40; Gamal: column 7, lines 40-45) wherein said traversing backward comprises:

starting with said clock period minus said setup delay at an exempt sequential cell; for each node traversed backward, subtracting a gate delay and assigning a lowest delay result value to said each node; and continuing to traverse backward only if said value is greater than said node's aggregate maximum delay (Gamal: column 7, lines 40-45).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571) 272-3749. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

July 5, 2005

Paul L. Rodriguez 7/8/05

Primary Examiner
Art Unit 2125

THS